ABSTRACT OF THE DISCLOSURE

The present invention provides a multi-phase-locked loop without dead zone, which can reduce clock jitter and provide larger tolerance for data random jitter. It generates and output multiple sets of control signals (up_k/dn_k) via a multi-phase voltage controlled oscillator which generates a plurality of multi-phase clock signals for detecting the transition edge of data signal. Therefore, the phase error θ_e and the voltage Vd of the multi-phase-locked loop can be adjusted to be nearly linear according to the control signals. A multi-phase-locked loop without dead zone thus can be provided.